Electronic Version
Stylesheet Version v1.1.1

NON-VOLATILE MEMORY CELL

Abstract

A memory cell includes an N-type well, three P-type doped regions, a first stacked dielectric layer, a first gate, a second stacked dielectric layer, and a second gate. The three P-type doped regions are formed on the N-well. The first dielectric stack layer is formed on the N-type well and between the first doped region and the second doped region from among the three P-type doped regions. The first gate is formed on the first stacked dielectric layer. The second stacked dielectric layer is formed on the N-type well and between the second doped region and the third doped region from among the three P-type doped regions. The second gate is formed on the second stacked dielectric layer.